e2v

DMUX 8-/10-bit 1:4/1:1.5 Gsps TSEV81102G0 Evaluation Board

User Guide

Table of Contents

e2v

Section 1
Overview

1.1 Features

- **50Ω Input Clock and Data (Differential ECL) through 2.54 mm Pitch Connectors**
- **Demultiplexed Outputs (Single-ended ECL) 50Ω Adapted on up to 8 x 2.54 mm Pitch Connectors**
- **DMUX Functions Adjusted by Jumpers and Potentiometers**
- **Separated Ground and Supplies**
- **Suitable for High-frequency Evaluation (up to 1.5 GHz)**
- **Board Dimensions: 200 mm x 190 mm**
- **Fully Assembled and Tested**

For optimal understanding and use of this evaluation board, please refer to the TS81102G0 DMUX specification also.

1.2 Description

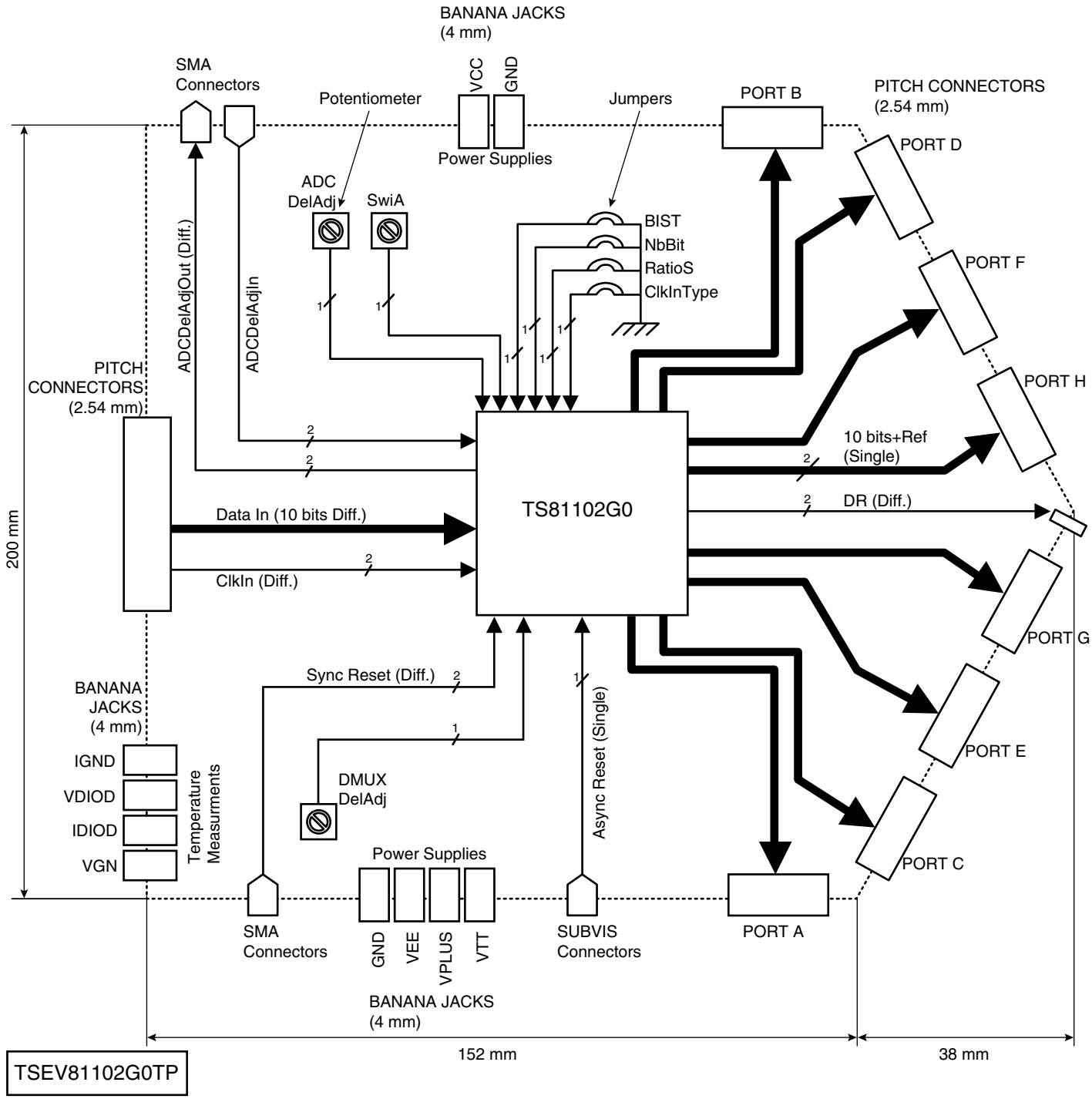
The TSEV81102G0 DMUX Evaluation Board (EB) is designed to simplify the characterization and the evaluation of the TS81102G0 device (1.5 Gsps DMUX). The DMUX EB enables the test of all the functions of the DMUX: Synchronous and Asynchronous reset functions, selection of the DMUX ratio (1:4 or 1:8), selection of the number of bits (8 or 10), output data common mode and swing adjustment, die junction temperature measurements over military temperature range, etc.

The DMUX EB has been designed to enable an easy connection with e2v ADC Evaluation Boards (i.e.: TSEV8388BG, TSEV83102G0) for an extended functionality evaluation (ADC+DMUX multi-channels applications).

The DMUX EB comes fully assembled and tested, with a TS81102G0 device implemented on-board and a heatsink assembled on the device.

1.3 TSEV81102G0 - Evaluation Board

Figure 1-1. TSEV81102G0 Block Diagram



0976F–BDC–02/09

1.4 Board Structure

1.4.1 Board Layers Thickness Profile

The TSEV81102G0 is a seven-layered PCB constituted by four copper layers and three dielectric layers.

The board is 1.75 mm thick.

The board layer's number, thickness, and functions are given below, from top to bottom.

Table 1-1. Board Layers Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 35 µm Input signals: 50Ω microstrip lines Output data signals: 60Ω microstrip lines, 50Ω terminated
Layer 2 RO4003 dielectric layer (Hydrocarbon/Wovenglass)	Layer thickness = 200 µm Dielectric constant = 3.4 at 10 GHz –0.044 dB/inch insertion loss at 2.5 GHz –0.318 dB/inch insertion loss at 18 GHz
Layer 3 Copper layer	Copper thickness = 35 µm Upper reference plane, divided in two parts: GND and V_{PLUSD}
Layer 4 BT/Epoxy dielectric layer	Layer thickness = 0.4 mm
Layer 5 Copper layer	Copper thickness = 35 µm Power plane: V_{EE}, V_{CC}, V_{TT}, GND
Layer 6 BT/Epoxy dielectric layer	Layer thickness = 1.0 mm
Layer 7 Copper layer	Copper thickness = 35 µm Lower reference plane (replica of layer 3)

1.4.2 Metal Layers

The four metal layers respectively correspond to: the signals' layer (layer 1), the two reference layers (layer 3 and layer 7) and the supply layer (layer 5).

The upper and the lower reference planes (layer 3 and 7) are partitioned into GND (reference for input signals) and V_{PLUSD} (reference for digital output signals), according to the same partition of the DMUX package.

Layer 5 is dedicated to power supplies (and ground).

1.4.3 Dielectric Layers

The three dielectric layers are respectively constituted by a low insertion loss dielectric (RO4003) layer (layer 2) and by a BT/Epoxy dielectric layer (layer 4 and 6).

Considering the severe mechanical constraints due to the wide temperature range and the high frequency domain in which the board is to operate, two different dielectric materials are used:

- The low insertion loss RO4003 Hydrocarbon/Wovenglass dielectric (–0.044 dB/inch loss at 2.5 GHz) which has an enhanced dielectric consistency in the high frequency domain is dedicated to the routing of 50Ω and 60Ω traces. The RO4003 dielectric constant is typically 3.4 at 10 GHz.
- The BT/Epoxy layer is chosen because of its enhanced mechanical characteristics for elevated temperature operations. The typical dielectric constant is 4.5 at 1 MHz. The BT/Epoxy dielectric has enhanced characteristics compared to FR4 Epoxy dielectric, namely:
  - higher operating temperature value: 170° C (125° C for FR4),
  - better withstanding of thermal shocks (from –65° C up to 170° C).

The characteristics of these two dielectrics make the board particularly suitable for performing measurements in the high frequency domain and over the military temperature range.

1.5 Power Supplies and Ground Access

The power supplies and ground access are provided by four 4 mm section banana jacks (red jacks) respectively for V_{EE}, V_{CC}, V_{TT}, V_{PLUSD}.

The Ground access is provided by two 4 mm banana jacks (black jacks).

Note: Two distinct Ground pads GND have been implemented on the board because of layout considerations. For proper use, connect them together to the same Ground.

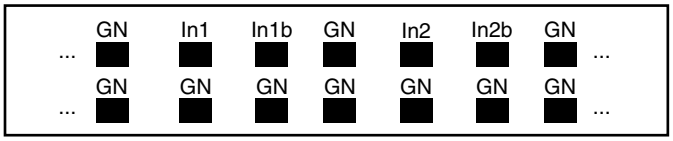
1.6 Input Access

1.6.1 Input Data and Clock Access

Access to the differential data and clock inputs (ClkIn, ClkInb, I[0..9], I[0..9]b) are provided by a female 2.54 mm pitch connector, via 50Ω microstrip lines.

The connector is made of 2 rows of pitches. The lower row is connected to GND. The upper row is used for the data and the clock connections. Each differential signal is separated by a pitch connected to GND, as shown:

Figure 1-2. Input Data Pitch Connector



Note: 100Ω differential adaptation is performed on-chip.

1.6.2 Synchronous Reset Access

Access to the signals SyncReset and SyncResetb is provided by two SMA connectors, via 50Ω microstrip lines.

Note: 100Ω differential adaptation is performed on-chip.

1.6.3 Asynchronous Reset Access

Access to the signal AsyncReset is provided by a SUBVIS connector.

1.6.4 ADC Synchronization Input Signal Access

Access to the differential signal ADCDELADJIN is provided by two SMA connectors, via 50Ω microstrip lines.

Note: 100Ω differential adaptation is performed on-chip.

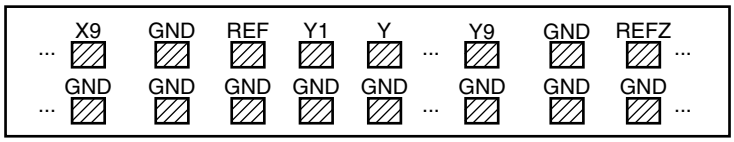
1.7 Outputs Access

1.7.1 Digital Outputs

Access to the single-ended output data and to the differential output clock (A[0..9] to H[0..9], RefA to RefH, DR, DRb) is provided by male 2.54 mm pitch connectors, via 60Ω microstrip lines. The microstrip lines are 50Ω terminated.

The connectors are made of 2 rows of pitches. The upper rows are used for the signals' connections. The lower rows are connected to GROUND. The output ports are separated from one another by a column (2 pitches) connected to GROUND, as shown:

Figure 1-3. Output Data Pitch Connector



Note: The characteristic impedance of the data output microstrip lines has been chosen to be 60Ω in order to terminate the lines either by 50Ω (ECL/PECL output format) or 75Ω resistors (TTL output format, available on request only).

1.7.2 ADC Synchronization Output Signal Access

Accesses to the differential signal ADCDELADJOUT are provided by two SMA connectors, via 50Ω microstrip lines.

1.8 DMUX Functions Settings

Four 2 mm-section banana jacks are provided to perform die temperature measurements (see Section 4.3).

Three potentiometers are provided for the adjustment of SWIADJ, ADCDELADJCTRL and DMUXDELADJCTRL respectively.

Four jumpers are provided for the setting of the static control signals NBBIT, RATIOSEL, CLKINTYPE and BIST (jumper on board = logic 0).

0976F–BDC–02/09

e2v

Section 2

Layout Information

Because the DMUX processes high-frequency signals, special attention was given to the board layout in order to achieve full speed operation efficiency. Thus, special effort was made in order to match the length of transmission lines for both input and output signals. In addition, cross-talk effects were reduced by increasing, wherever possible, the space between the lines.

2.1 Power Supplies Decoupling

Each power supply is bypassed by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor.

Each power supply access of the DMUX is also bypassed as close as possible to the device, by a 10 nF and a 100 pF surface mount chip capacitor in parallel.

Note: Those capacitors are superposed.

2.2 Reference Planes

Each reference plane (layer 3 and layer 7) is physically divided in two parts: one GND trace and one V_{PLUSD} trace, which is the voltage reference of the output buffers of the DMUX. V_{PLUSD} can be set to GND (ECL format) or to 3.3V (PECL/TTL format) according to the desired output format.

2.3 I/O Transmission Lines

The following table summarizes the main properties of the microstrip lines of all the input and output signals. Note that the transmission delay through a transmission line is approximately 6.1 ps/mm.

Table 2-1. I/O Transmission Lines

Signal	Type	Typical Length	Length Matching	Characteristic Impedance	Adaptation	Comments
ClkIn ClkInb	Differential	69 mm 69.7 mm	– –	50Ω 50Ω	On-chip 100Ω diff.	
I[0..9], I[0..9]b	Differential	68.8 mm	±1	50Ω	On-chip 100Ω diff.	Min length (I3): 67.8 mm Max length (I9): 69.6 mm
A[0..9], ..., H[0..9]	Single	111.4 mm	±8	60Ω	50Ω	Min length (F3 & E5): 104.2 mm Max length (C9): 119.3 mm
DR DRb	Differential	111.9 mm 114.5 mm	– –	60Ω 60Ω	50Ω 50Ω	
SyncReset, SyncResetb	Differential	96 mm	±1	50Ω	On-chip 100Ω diff.	
ADCDELADJIN, ADCDELADJINb	Differential	104 mm	±1	50Ω	On-chip 100Ω diff.	
ADCDELADJOUT, ADCDELADJOUTb	Differential	111 mm	±1	50Ω	None	

Note: Two ground accesses, OSC1 and OSC2, have been provided near the DMUX for measurements purposes.

0976F–BDC–02/09

e2v

Section 3

DC Characteristics and Current Consuption

3.1 Operating Charcteristics

In this section, the typical values of the board's I/O signals and power sources are listed. These values refer to a nominal use of the evaluation board. These values are purely indicative and may depend on temperature, frequency of use, etc.

The following tables give an estimation of the power consumption of the board, including the current consumption of DMUX and the current consumption induced by the components added on the board.

The values given below are relevant for ECL 50Ω, PECL 50Ω and TTL 75Ω output formats only, assuming that the DMUX is working in ratio 1:8, 10 bits.

For further information about output formats, please also refer to Section 4.3.

Table 3-1. Supply Voltage

Parameter	ECL 50Ω	PECL 50Ω	TTL 75Ω	Unit
V_{CC}	5	5	5	V
V_{PLUSD}	0	3.3	3.3	V
V_{TT}	–2	1.3	0.25	V
V_{EE}	–5	–5	–5	V

Table 3-2. Output Voltage (at T = 125° C)

Parameter	ECL 50Ω	PECL 50Ω	TTL 75Ω	Unit
V_{OL}	–1.8	1.5	0.5	V
V_{PH}	–0.8	2.5	2.5	V
V_{REF}	–1.3	2.0	1.5	V

Table 3-3. Maximum Current Consumption

Parameter	ECL 50Ω (SWIADJ = 0V)	PECL 50Ω (SWIADJ = 0V)	TTL 75Ω (SWIADJ = 0.5V)	Unit
I_{CC}	40	40	40	mA
I_{PLUSD}	2200	2200	3010	mA
I_{TT}	1940	1940	2630	mA
I_{EE}	800	800	880	mA

3.2 Electrical Characteristics

The following table lists the absolute maximum values of the board. These maximum ratings are limiting values to be considered individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect the DMUX reliability.

Table 3-4. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Positive output buffer supply voltage	V_{PLUSD}		GND to 4	V
Negative supply voltage	V_{EE}		GND to –6	V
Analog input voltages	ADCDelAdjCtrl, ADCDelAdjCtrlb or DMUXDelAdjCtrl, DMUXDelAdjCtrlb or SwiAdj	Voltage range for each pad Differential voltage range	0 to 1 –1 to 1	V
ECL 50Ω input voltage	Clkln or Clklnb or I[0…9] or I[0…9]b or SyncReset or SyncResetb or ADCDelAdjln or ADCDelAdjlnb	Voltage range for each pad	–2.2 to 0.6	V
Maximum difference between ECL 50Ω input voltages	Clkln – Clklnb or I[0…9] - I[0…9]b or SyncReset – Syncresetb or ADCDelAdjln - ADCDelAdjlnb	Minimum differential swing Maximum differential swing	0.1 2	V
Data output current	A[0…9] to H[0…9] or RefA to RefH or DR or DRb	Maximum current	36	mA
TTL input voltages	Clkln Type RatioSel NbBit AsyncReset BIST		GND to V_{CC}	V
Maximum input voltage on diode for temperature measurement	DIODE		700	mV
Maximum input current on diode	DIODE		8	mA
Maximum junction temperature	T_j		135	°C
Storage temperature	T_{stg}		–65 to 150	°C

Note: Absolute maximum ratings are limiting values, to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. The use of a thermal heat sink is mandatory.

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Section 4

Main Function Description

4.1 Introduction

Other function descriptions are available in the TS81102G0 DMUX datasheet.

4.2 Quick Start

The evaluation board is delivered fully assembled and tested. A heatsink, which is strongly recommended, is also delivered assembled.

Do not turn on the power supplies until all power connections to the evaluation board are established.

The procedure described below aims at helping when the board is used for the first time. It describes the steps to accomplish a BIST test (Built-In Self Test, see Section 4.6) in order to verify whether the board is functional or not. At the end of the procedure, the DMUX will be in the following configuration: DR mode, 10 bits mode, 1:8 ratio, BIST activated, SWIADJ = 0V, ECL output format.

1. Connect the board's ground pads together.
2. Connect the pad marked V_{PLUSD} to the GND pad.
3. Connect a –5V power supply source to the pad marked V_{EE}. Then, connect the supply's ground to the GND pad.
4. Connect a +5V power supply source to the pad marked V_{CC}. Then, connect the supply's ground to the GND pad.
5. Connect a –2V power supply source to the pad marked V_{TT}. Then, connect the supply's ground to the GND pad.
6. Connect your input clock to the board (pitches CLKIN and CLKINB). This clock may either be differential or single-ended (see Section 4.4).
7. Remove the jumpers marked NBBIT and CLKINTYPE. The remaining jumpers are RATIOSEL and BIST.
8. Connect a logic analyzer, such as an HP16500 at the output of the board.
9. Turn on the supply and signal sources according to the following sequence:
   - V_{EE} first
   - V_{CC}
   - V_{PLUSD}
   - V_{TT}
   - Input clock

10. Set the potentiometer marked SWIADJ such that the voltage on the SWIADJ pin of the DMUX is 0V.
11. Connect pad ASYNCRESET to ground (the ASYNCHRESET is active at TTL high level and must be tied to ground when the device is running).

At the output, the demultiplexed BIST sequence shall be observed.

Note: It is not necessary to verify the 512 codes of the BIST to make sure that the DMUX is functional. Verifying the first 16 codes is indeed sufficient.

4.3 DMUX Settings Adjustment

Four jumpers are provided in order to activate the functions RATIOSEL, BIST, CLKINTYPE and NBBIT. When the jumper is on-board, it corresponds to logic 0. The following table recapitulates which functions are active when the jumpers are on-board or not.

Table 4-1. DUMX Settings Adjustment

Name	Jumper	Function
CLKINTYPE	ON	DR/2 mode
	OUT	DR mode
BIST	ON	BIST active
	OUT	BIST inactive
NBBIT	ON	8 bits mode
	OUT	10 bits mode
RATIOSEL	ON	1:8 DMUX Ratio
	OUT	1:4 DMUX Ratio

4.4 BIST

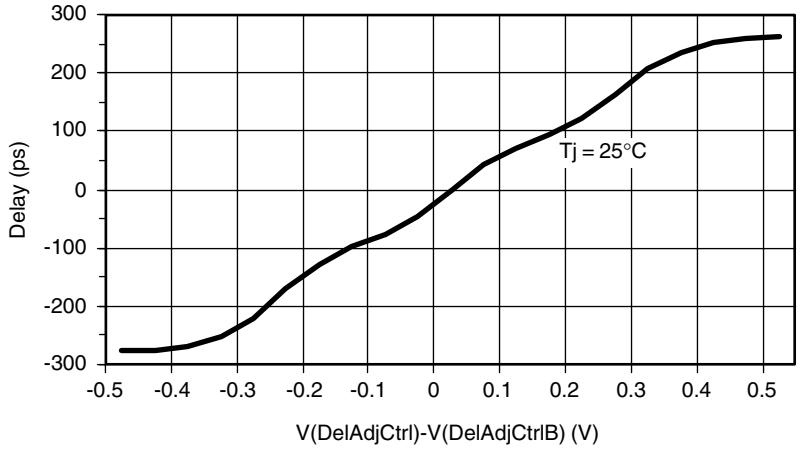
A pseudo-random 10-bit generator is implemented in the DMUX. It generates a 10 bits signal at the output of the DMUX, with a period of 512 input clock's periods. The sequence start on port A. The output obtained on port A to H depends on the conversion ratio. The driving clock of BIST is ClkIn. CLKINTYPE must be set to logic 1 (jumper out) to have different 10-bit code on each output. The complete BIST sequence is available on request.

4.5 Delay Adjust

Two delay adjusts of ±250 ps, controlled by potentiometers, are available in order to synchronize the input clock and data of the DMUX on the one hand, and to delay the signal ADCDELADJIN on the other hand.

- The input DelAdjCtrl has been set to 0V.
- The input DelAdjCtrlb varies from –0.55V to 0.55V, according to the potentiometer position.
- The generated delay is proportional to the differential voltage V(DelAdjCtrl)–V(DelAdjCtrlb) as shown in the next graph (Figure 4-1).

Figure 4-1. Delay Adjustment Characteristic



Note: The variation of the delay in function of the temperature is insignificant.

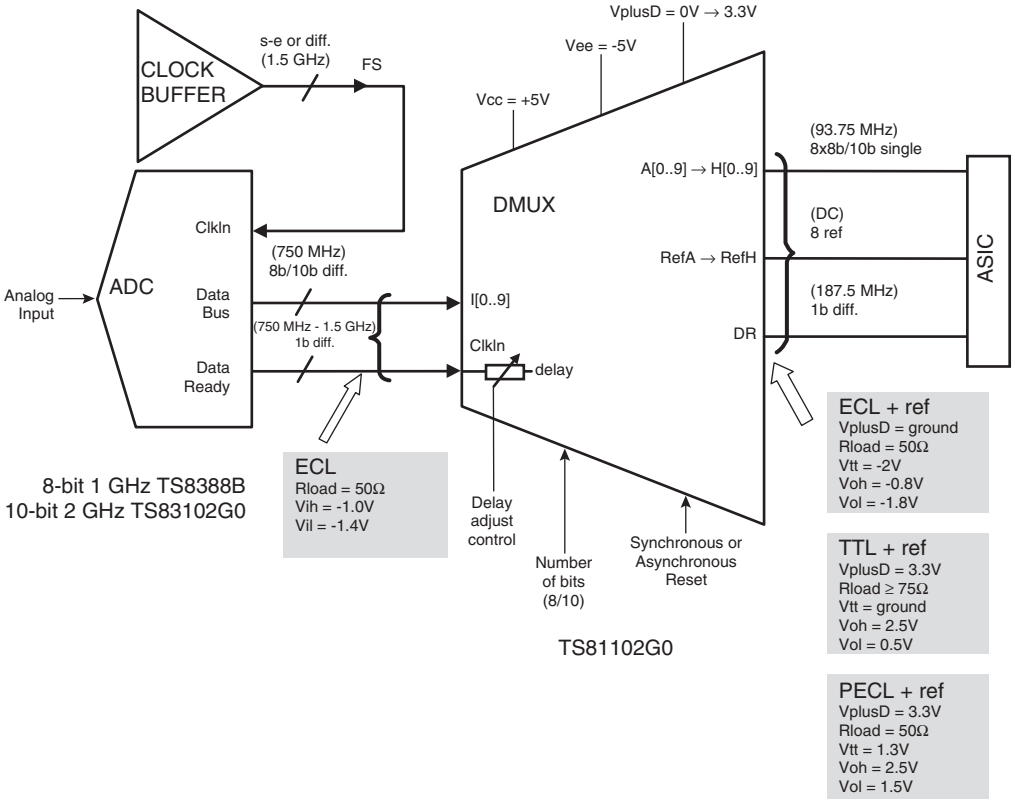
4.6 Miscellaneous

- Always wear an anti-static strap when manipulating the board, the DMUX being very sensitive to ESDs.
- Make sure that the current as delivered by your power supplies is sufficient to supply the board.
- Always switch on the DMUX board supplies in the following order: V_{EE} first, V_{CC}, V_{PLUSD} and V_{TT}.
- Always make sure that the output current through the termination resistors does not exceed 36 mA.
- After the supplies are switched on, send an asynchronous reset pulse into the DMUX (i.e. leave the pad ASYNCRESET open and then connect it to the ground).

4.7 Applying the TSEV81102G0 DMUX

The TSEV81102G0 DMUX evaluation board has been designed to be connected with TSEV8388B and TSEV83102G0 ADC evaluation boards.

Figure 4-2. TSEV81102G0 DMUX Evaluation Boards



Please, refer to the specific document "DMUX and ADC APPLICATION NOTES" for more information.

4.8 ADC to DMUX Connections

The DMUX inputs configuration has been optimized to be connected to the TS8388B ADC.

The die in the TBGA package is up. For the ADC, different types of packages can be used such as CBGA with die up or the CQFP68 with die down. The DMUX device being completely symmetrical, both ADC packages can be connected to the TBGA package of the DMUX without crisscrossing the lines (see table below).

Table 4-2. ADC to DMUX Connections

ADC Digital Outputs CQFP68 Package	DMUX Data Inputs TBGA Package	ADC Digital Outputs CBGA Package	DMUX Data Inputs TBGA Package
D0	I7	D0	I0
D1	I6	D1	I1
D2	I5	D2	I2
D3	I4	D3	I3
D4	I3	D4	I4
D5	I2	D5	I5
D6	I1	D6	I6
D7	I0	D7	I7
–	18 not connected	–	18 not connected
–	19 not connected	–	19 not connected

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Section 5

Package Description

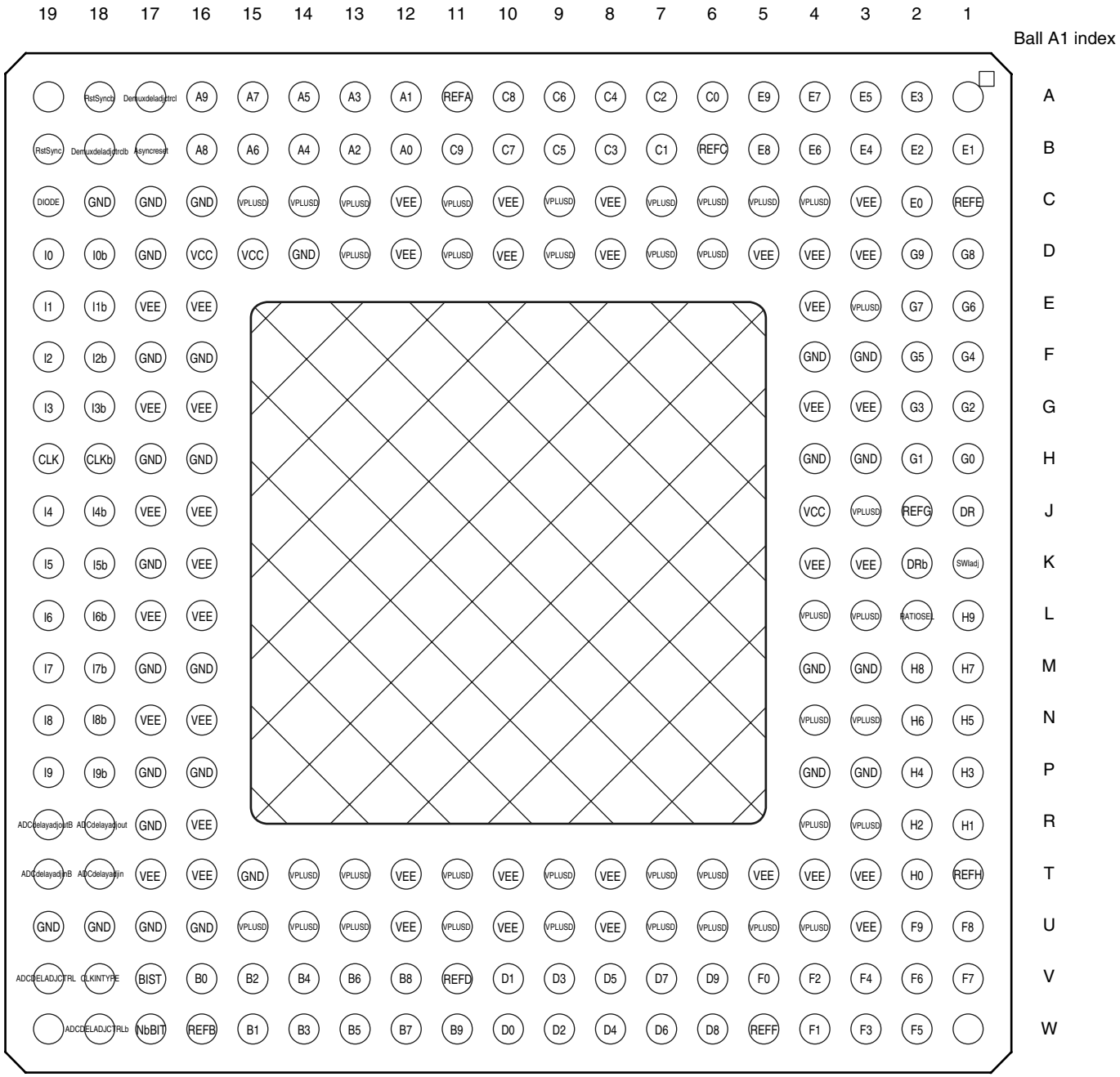
5.1 Introduction

Information in this section is extracted from the TS81102G0 DMUX datasheet. For exhaustive information about the device's package, please refer to its datasheet.

0976F–BDC–02/09

5.2 TS81102G0 Pinout

Figure 5-1. TS81102G0 Pinout of TBGA 240 Package



0976F–BDC–02/09

Table 5-1. TSEV81102G0 Pin Description

Type	Name	Levels	Comments
Digital Inputs	I[0…9]	Differential ECL	Data input.
	ClkIn	Differential ECL	Clock input.
Outputs	A[0…9] →H[0…9]	Adjustable Logic Single	Data output for channel A to H. Common mode is adjusted with V_{PLUSD}. Swing is adjusted with SwiAdj.
	DR	Adjustable Logic Single	Data output for channel A to H. Common mode is adjusted with V_{PLUSD}. Swing is adjusted with SwiAdj.
	RefA →RefH	Adjustable Single	Reference voltage for channels A to H. Common mode is adjustable with V_{PLUSD}.
Control Signals	ClkInType	TTL	Mode DR or DR/2 (logic 1: Data Ready).
	RatioSel	TTL	DMUX ratio (logic 1: 1:4).
	Bist	TTL	BIST selection (logic 0: BIST active).
	SwiAdj	0V ± 0.5V	Swing fine adjustment of output buffers.
	Diode	Analog	Diode for chip temperature measurement.
	NbBit	TTL	Number of bits: 8 or 10 (logic 1: 10 bits).
Synchronization	AsyncReset	TTL	Asynchronous reset (logic 1: reset on).
	SyncReset	Differential ECL	Synchronous reset (on rising edge).
	DMUXDelAdjCtrl	Differential analog input of ± 0.5V	Control of the delay line of DataReady input: Differential input = –0.5V, delay = 250 ps Differential input = 0V, delay = 500 ps Differential input = 0.5V, delay = 750 ps
	ADCDelAdjCtrl	Differential analog input of ± 0.5V	Control of the delay line for ADC: Differential input = –0.5V, delay = 250 ps Differential input = 0V, delay = 500 ps Differential input = 0.5V, delay = 750 ps
	ADCDelAdjIn	Differential ECL	Stand-alone delay adjust input for ADC. Differential termination of 100Ω inside the buffer.
	ADCDelAdjOut	50Ω differential output	Stand-alone delay adjust output for ADC.
Power Supplies	GND	Ground 0V	Common ground.
	V_{EE}	Power –5V	Digital negative power supply.
	V_{PLUSD}	Adjustable power from 0V to +3.3V	Common mode adjustment for output buffers.
	V_{CC}	Power +5V	Digital positive power supply.

Table 5-2. TBGA 240 Package

Row	Col	Name	Row	Col	Name	Row	Col	Name	Row	Col	Name
A	1	NC	D	4	VEE	K	16	VEE	T	17	VEE
A	2	E3	D	5	VEE	K	17	GND	T	18	ADCDELADJIN
A	3	E5	D	6	VPLUSD	K	18	I5B	T	19	ADCDELADJINB
A	4	E7	D	7	VPLUSD	K	19	I5	U	1	F8
A	5	E9	D	8	VEE	L	1	H9	U	2	F9
A	6	C0	D	9	VPLUSD	L	2	RATIOSEL	U	3	VEE
A	7	C2	D	10	VEE	L	3	VPLUSD	U	4	VPLUSD
A	8	C4	D	11	VPLUSD	L	4	VPLUSD	U	5	VPLUSD
A	9	C6	D	12	VEE	L	16	VEE	U	6	VPLUSD
A	10	C8	D	13	VPLUSD	L	17	VEE	U	7	VPLUSD
A	11	REFA	D	14	GND	L	18	I6B	U	8	VEE
A	12	A1	D	15	VCC	L	19	I6	U	9	VPLUSD
A	13	A3	D	16	VCC	M	1	H7	U	10	VEE
A	14	A5	D	17	GND	M	2	H8	U	11	VPLUSD
A	15	A7	D	18	I0B	M	3	GND	U	12	VEE
A	16	A9	D	19	I0	M	4	GND	U	13	VPLUSD
A	17	DEMUXDELADJCTRL	E	1	G6	M	16	GND	U	14	VPLUSD
A	18	RSTSYNCB	E	2	G7	M	17	GND	U	15	VPLUSD
A	19	NC	E	3	VPLUSD	M	18	I7B	U	16	GND
B	1	E1	E	4	VEE	M	19	I7	U	17	GND
B	2	E2	E	16	VEE	N	1	H5	U	18	GND
B	3	E4	E	17	VEE	N	2	H6	U	19	GND
B	4	E6	E	18	I1B	N	3	VPLUSD	V	1	F7
B	5	E8	E	19	I1	N	4	VPLUSD	V	2	F6
B	6	REFC	F	1	G4	N	16	VEE	V	3	F4
B	7	C1	F	2	G5	N	17	VEE	V	4	F2
B	8	C3	F	3	GND	N	18	I8B	V	5	F0
B	9	C5	F	4	GND	N	19	I8	V	6	D9
B	10	C7	F	16	GND	P	1	H3	V	7	D7
B	11	C9	F	17	GND	P	2	H4	V	8	D5
B	12	A0	F	18	I2B	P	3	GND	V	9	D3
B	13	A2	F	19	I2	P	4	GND	V	10	D1
B	14	A4	G	1	G2	P	16	GND	V	11	REFD
B	15	A6	G	2	G3	P	17	GND	V	12	B8
B	16	A8	G	3	VEE	P	18	I9B	V	13	B6
B	17	ASYNCRESET	G	4	VEE	P	19	I9	V	14	B4
B	18	DEMUXDELADJCTRLB	G	16	VEE	R	1	H1	V	15	B2
B	19	RSTSYNC	G	17	VEE	R	2	H2	V	16	B0
C	1	REFE	G	18	I3B	R	3	VPLUSD	V	17	BIST
C	2	E0	G	19	I3	R	4	VPLUSD	V	18	CLKINTYPE
C	3	VEE	H	1	G0	R	16	VEE	V	19	ADCDELADJCTRL
C	4	VPLUSD	H	2	G1	R	17	GND	W	1	NC
C	5	VPLUSD	H	3	GND	R	18	ADCDELADJOUT	W	2	F5
C	6	VPLUSD	H	4	GND	R	19	ADCDELADJOUTB	W	3	F3
C	7	VPLUSD	H	16	GND	T	1	REFH	W	4	F1
C	8	VEE	H	17	GND	T	2	H0	W	5	REFF
C	9	VPLUSD	H	18	CLKINB	T	3	VEE	W	6	D8
C	10	VEE	H	19	CLKIN	T	4	VEE	W	7	D6
C	11	VPLUSD	J	1	DR	T	5	VEE	W	8	D4
C	12	VEE	J	2	REFG	T	6	VPLUSD	W	9	D2
C	13	VPLUSD	J	3	VPLUSD	T	7	VPLUSD	W	10	D0
C	14	VPLUSD	J	4	VCC	T	8	VEE	W	11	B9
C	15	VPLUSD	J	16	VEE	T	9	VPLUSD	W	12	B7
C	16	GND	J	17	VEE	T	10	VEE	W	13	B5
C	17	GND	J	18	I4B	T	11	VPLUSD	W	14	B3
C	18	GND	J	19	I4	T	12	VEE	W	15	B1
C	19	DIODE	K	1	SWIADJ	T	13	VPLUSD	W	16	REFB
D	1	G8	K	2	DRB	T	14	VPLUSD	W	17	NBBIT
D	2	G9	K	3	VEE	T	15	GND	W	18	ADCDELADJCTRLB
D	3	VEE	K	4	VEE	T	16	VEE	W	19	NC

5.3 Thermal and Moisture Characteristics

5.3.1 Thermal Resistance from Junction to Case: RTHJC

The Rth from junction to case for the TBGA package is estimated at 0.7° C/W which can be decomposed in:

- Silicon: 0.1° C/W
- Die attach epoxy: 0.5° C/W (thickness # 50 µm)
- Copper block (back side of the package): 0.1° C/W.

5.3.2 Thermal Resistance from Junction to Ambient: RTHJA

A pin-fin type heatsink, size 40 mm x 40 mm x 8 mm can be used to reduce thermal resistance. This heatsink should not be glued on top of the package as e2v does not guarantee the attachment on the board in such a configuration. The heatsink could be clipped or screwed on the board.

With such a heatsink the Rthj-a is about 6° C/W. (If e2v takes 10° C/W for Rth through the heatsink in parallel with 15° C/W for Rth through the balls).

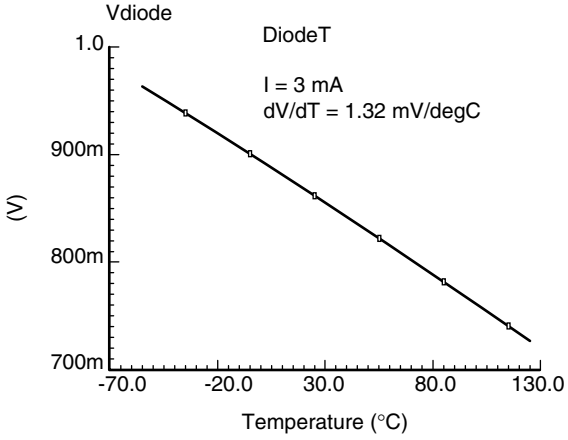
Without a heatsink, the Rth junction to air for a package reported on-board can be estimated from 13 to 20° C/W (depending on the board used).

The worst value 20° C/W is given for 1-layer board (13° C for 4-layer board).

5.3.3 Temperature Diode Characteristic

The theoretical characteristic of the diode, in function of the temperature when I = 3 mA is depicted below.

Figure 5-2. Temperature Diode Characteristic



5.3.4 Moisture Characteristic

This device is sensitive to the moisture (MSL3 according JEDEC standard).

Shelf life in sealed bag: 12 months at < 40° C and < 90% relative humidity (RH).

After this bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temperature 220° C) must be:

- mounted within 168 hours at factory conditions of ≤30° C/60% RH, or
- stored at ≤20% RH.

Devices require baking, before mounting, if Humidity Indicator is > 20% when read at 23° C ±5° C.

If baking is required, devices may be baked for:

- 192 hours at 40° C + 5° C/–0° C and < 5% RH for low temperature device containers, or
- 24 hours at 125° C ± 5° C for high-temperature device containers.

5.4 Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
TS81102G0VTP	TBGA 240	"V" grade: –40° C < Tc; Tj < 110° C	Standard	Contact e2v for availability
TS81102G0MFS	CQFP + HS	T_C > –55° C, T_J < 125° C		Contact e2v for availability
TSEV81102G0FS	Evaluation board	+25° C		Contact e2v for availability

Section 6

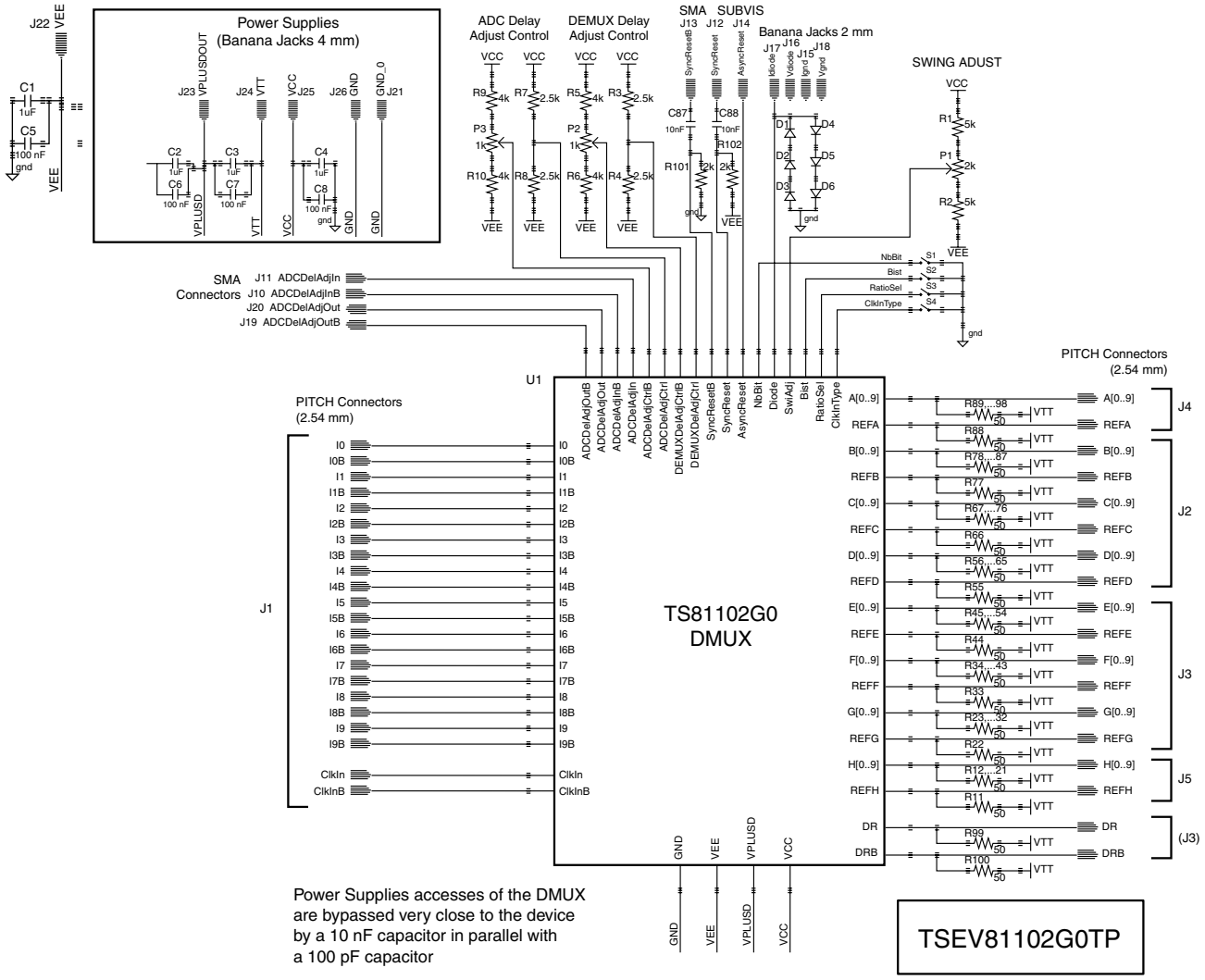
Schematics

6.1 TSEV81102G0 Electrical Schematic

Please, see the following figures.

0976F–BDC–02/09

Figure 6-1. TSEV81102G0 Electrical Schematic



6.2 Component List

Table 6-1. Component List

Type	Reference	Quantity	Label
SMA CONNECTOR	VITELEC 142 – 0701 – 851	2	J12, J13
	RADIALL R125 620 001	4	J10, J11, J19, J20
BANANA JACK 4 mm	DELTRON	6	J21 to J26
	E. F. JOHNSON	4	J15 to J18
SUBVIS CONNECTOR	RADIALL R112 665	1	J14
PITCH CONNECTOR 2.54 mm (two rows)	–	5	J1 to J5
CAPACITOR	CHIP TANTALE 1 uF, 20V	4	C1 to C4
	CHIP Ceramic 100 nF	4	C5 to C8
	CHIP Ceramic 10 nF	39	C9, C11, C13, C15, C17, C19, C21, C23, C25, C27, C29, C31, C33, C35, C37, C39, C41, C43, C45, C47, C49, C51, C53, C55, C57, C59, C61, C63, C65, C67, C69, C71, C73, C75, C77, C79, C81, C83, C85, C87, C88
	Ceramic 10 nF	39	C10, C12, C14, C16, C18, C20, C22, C24, C26, C28, C30, C32, C34, C36, C38, C40, C42, C44, C46, C48, C50, C52, C54, C56, C58, C60, C62, C64, C66, C68, C70, C72, C74, C76, C78, C80, C82, C84, C86
RESISTOR	CHIP 5 KΩ 1%	2	R1, R2
	CHIP 4 KΩ 1%	4	R5, R6, R9, R10
	CHIP 2.5 KΩ 1%	2	R3, R4, R7, R8
	CHIP 2 KΩ 1%	2	R101, R102
	CHIP 50Ω 1%	90	R11 to R100
POTENTIOMETER	BOURNS 2 KΩ 25 turns	1	P1
	BOURNS 1 KΩ 25 turns	2	P2, P3
DIODE	–	6	D1 to D6
DMUX	TS81102G0	1	U1

6.3 Evaluation Board Schematics

Figure 6-2. Component Side Description

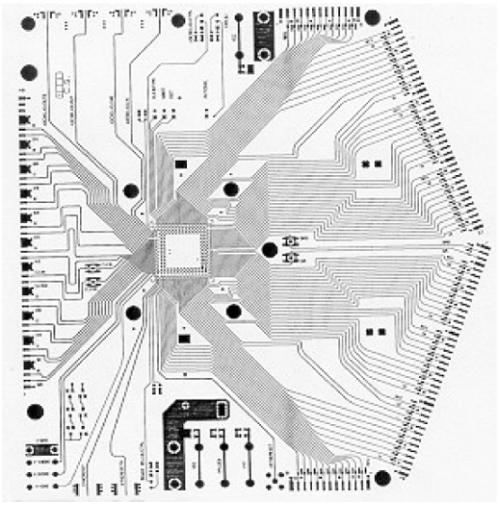


Figure 6-3. Reference Planes

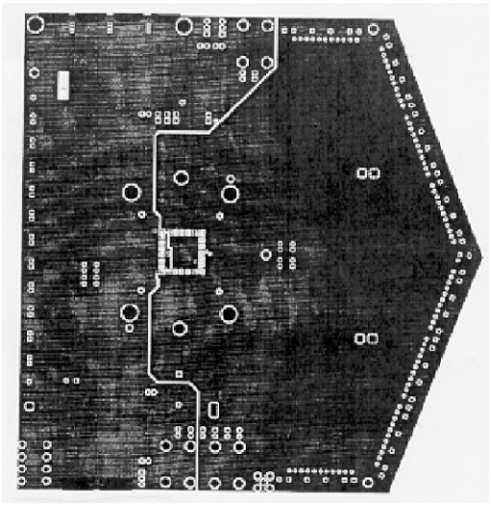
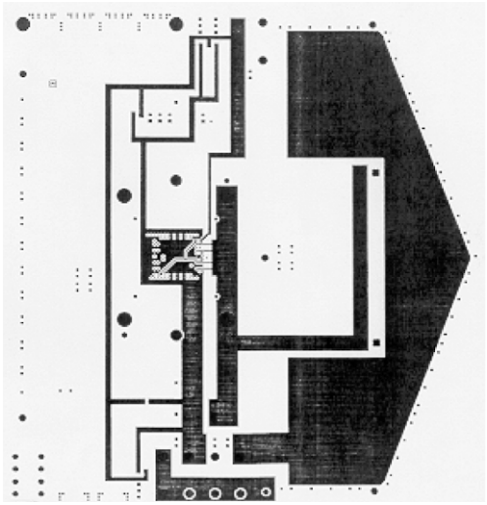


Figure 6-4. Power Supplies Plane



0976F–BDC–02/09

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